

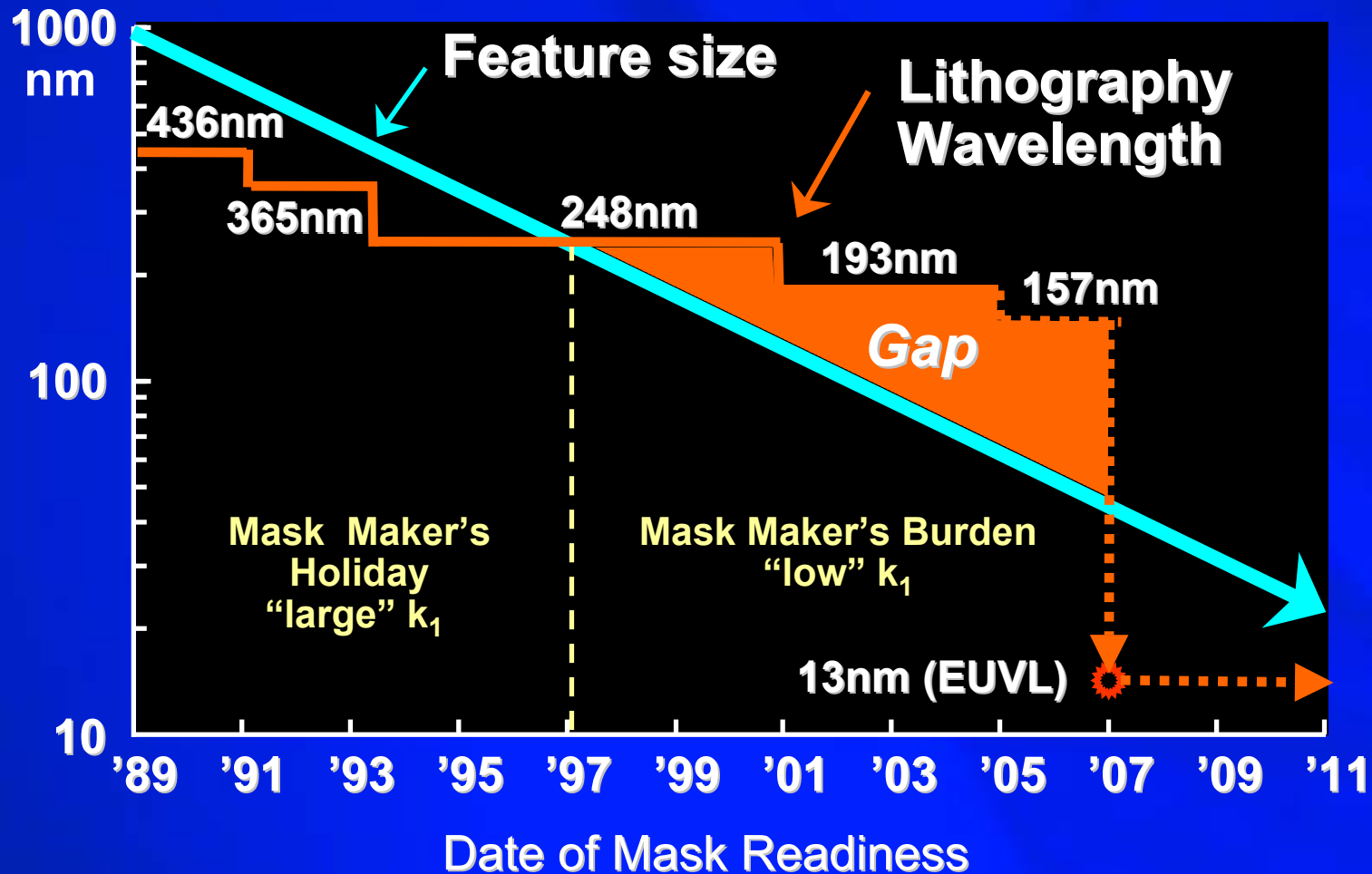
Intel EUV Mask Technology

Fu-Chang Lo, Ph.D.
Assistant Director
Components Research
Intel Corporation

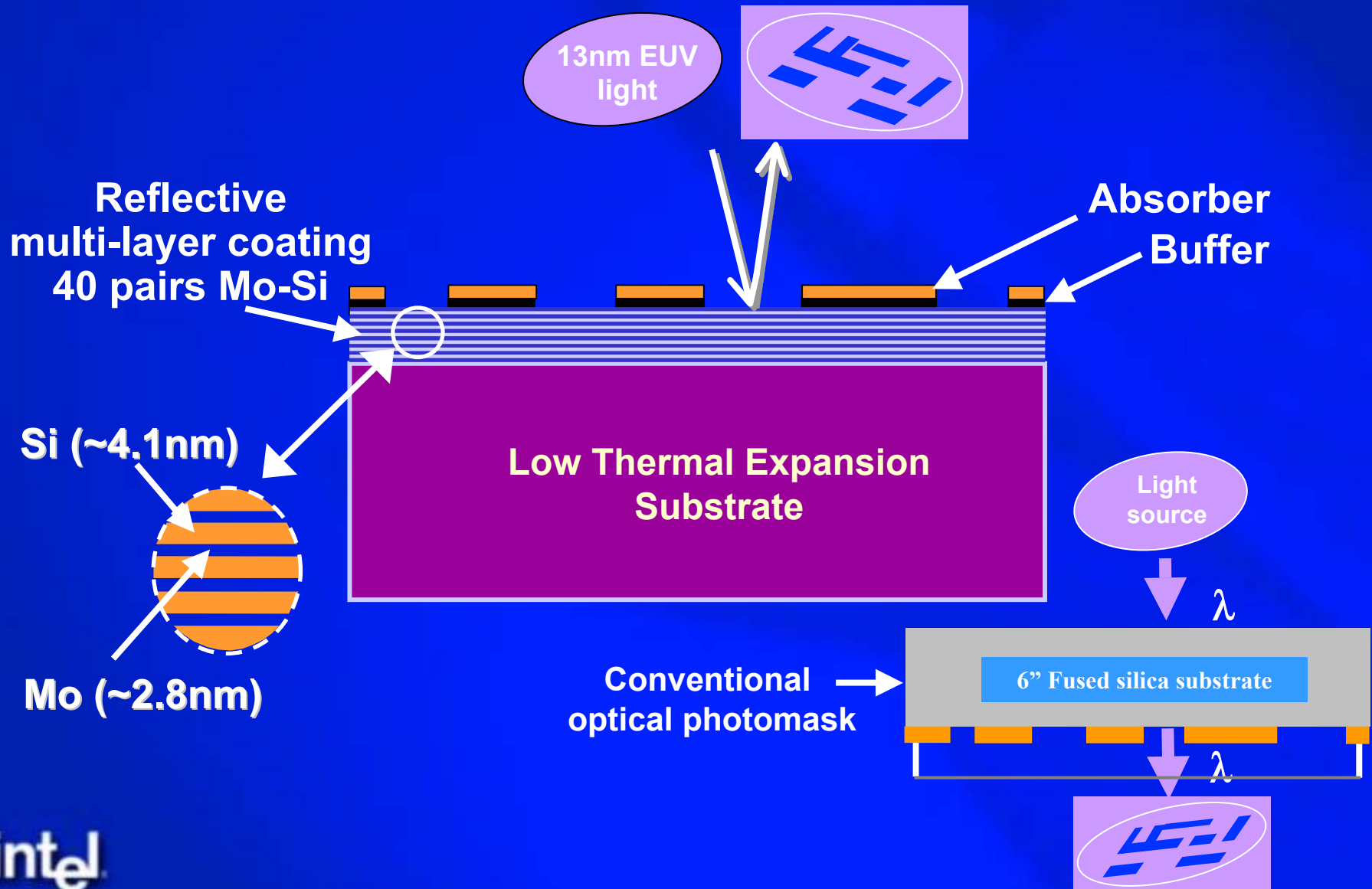
What Are We Disclosing Today?

- Intel has successfully fabricated EUV masks for 32 nm node generation.
- Through active efforts from Intel, commercial suppliers are providing blanks and tools for EUV mask making.
- Intel mask technology will allow Intel to be the first to deploy EUV lithography in high volume manufacturing, further extending Moore's law for another decade.

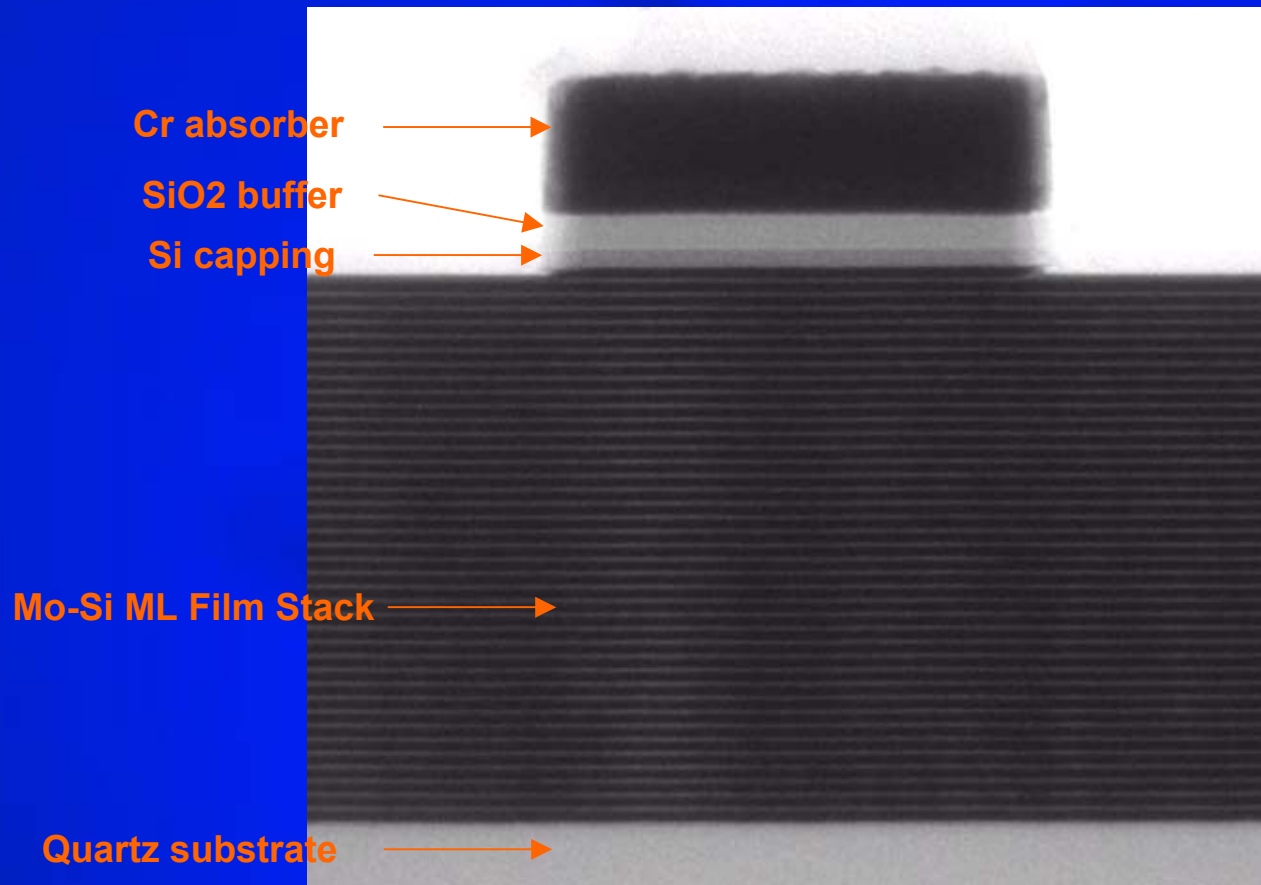
Intel Mask Technology Roadmap



EUV Reflective Mask Structure



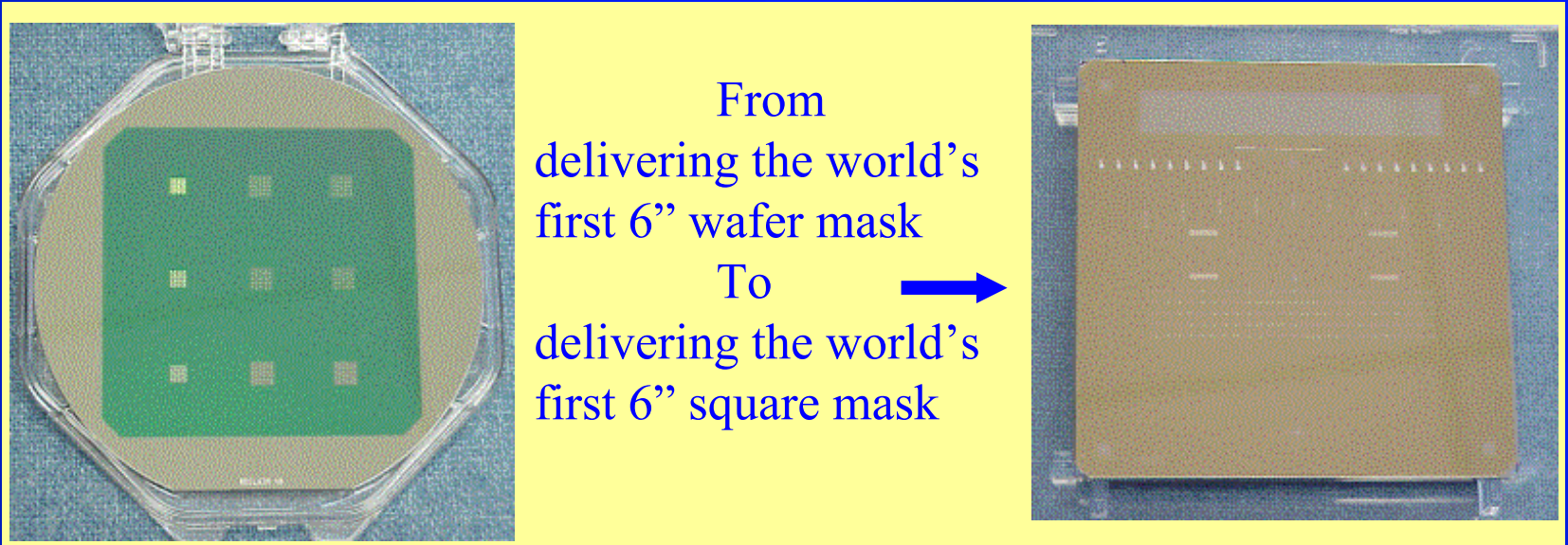
Cross Section of a Fully Fabricated Mask



Excellent absorber patterning!

Demonstrated EUV Mask Technology Leadership

- 32 patents
- 41 publications



6" square mask is compatible with current mask making equipment

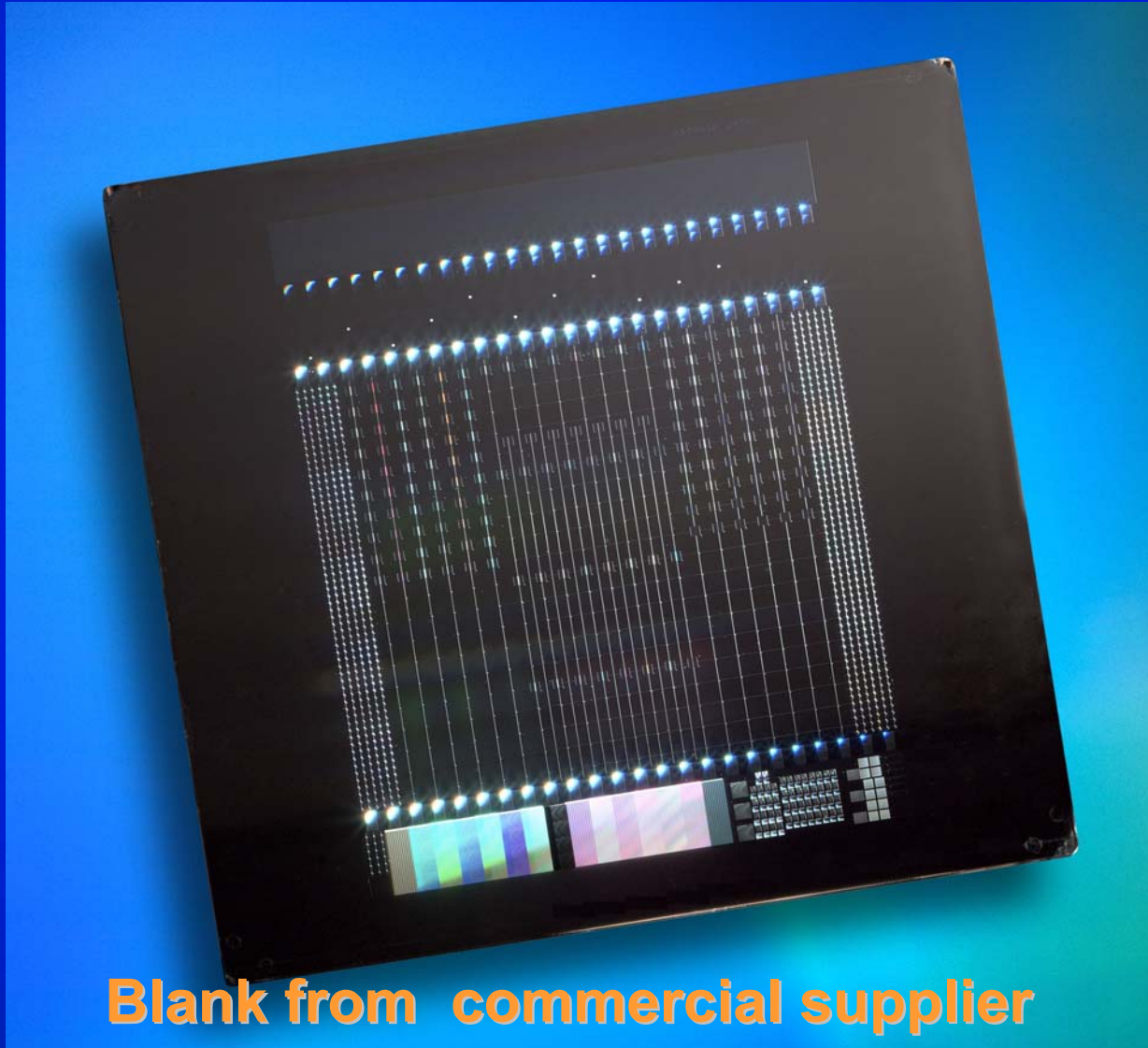
Now We Are in Competitive Phase

- Intel mask efforts will allow Intel to be the first to deploy EUV lithography

Our Parallel Focus:

- Develop critical in-house capabilities
 - Integrated solutions using internal superior mask making capabilities
 - New EUV mask specific capabilities
- Actively enable infrastructure development
 - Several potential substrate material and blank commercial suppliers
 - Multiple equipment tool suppliers

EUV Mask Fabricated at Intel Mask Shop



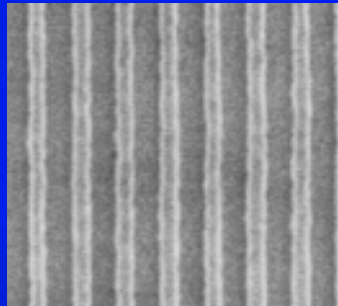
Blank from commercial supplier

EUV Mask Pattern Dimensions for 32 nm Node

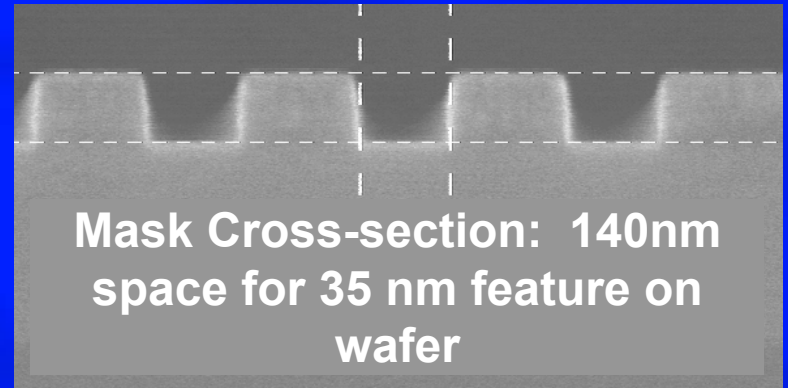
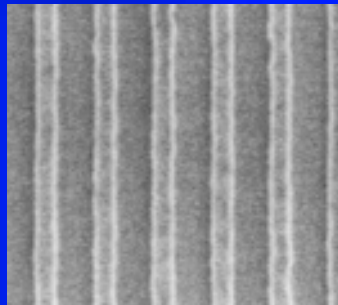
128 nm on Mask Needed for 32 nm on Wafer

Mask Top-down SEM
Micrographs

32nm node
120nm I/s (4X)

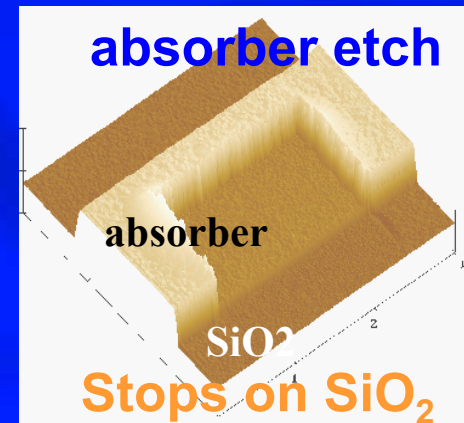
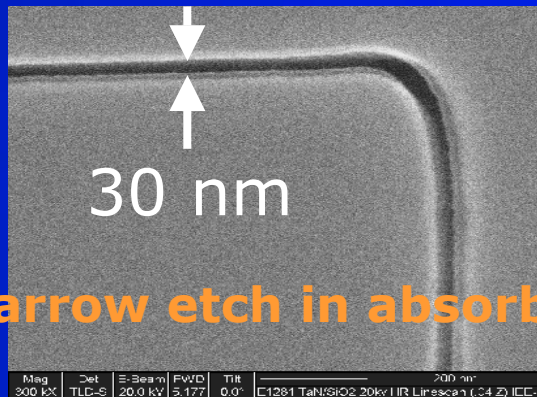


45nm node
200nm I/s (4X)

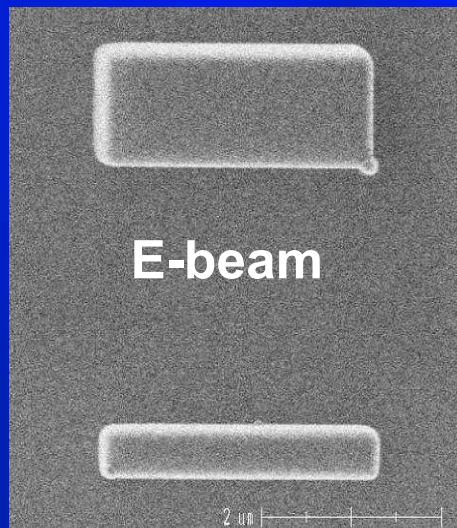


Intel Co-developed Damage-Free Mask Repair Technology Using Electron-beams

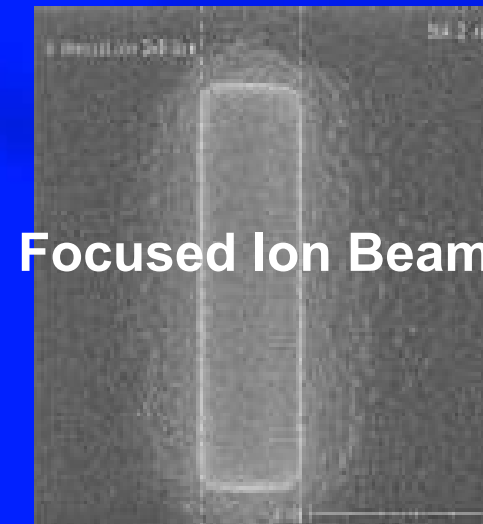
- High resolution
- No surface damage



- E-beam deposition shows no halo effect



vs.



Commercial EUV Mask Inspection Tool Development

- Intel active participation & early learning
- Can detect the equivalent of all 2 inch bumps over the area of California in 20 minutes.



- Detects 11nm high defects
- Tool available now

**Commercial EUVL
Inspection Tool**

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Summary

- Mask is a critical component of lithography that drives Moore's Law
- The low K_1 "Burden" drives mask complexity & cost
- Mask industry landscape has been undergoing vast changes
- Intel invests in internal mask shop providing major competitive advantages
 - Leading edge capabilities
 - Product introduction throughput time
 - Integrated solutions and services
 - Mask cost
- Intel is generating world leading 65nm node mask sets to continue the 2-year technology cycle
- Intel has announced plans to build a 500mm EUV mask production facility
 - Demonstrate 500mm EUV mask
 - Position for 7nm node insertion
 - Will extend mask life into next decade

